

Nanotechnology makes brighter LED's

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Outline

- Why are LED's such a big deal ?
 - Brightness; lumens per watt & lumens per dollar
 - Applications
- How does nanotechnology help ?
 - Light extraction
 - Light creation
- How to implement nanotechnology cost effectively ?
 - Sub 100 nm features at < 1 c per device
 - Limited align and defects
 - Ideal imprint application
 - Which companies are poised to make an impact ?

Why are LED's such a big deal ?

- **Light usage**

- \$230 B world wide – 30% savings possible, > 300 power plants + fuel.....

- | Light | efficiency | cost | life |
|----------------|-------------------|-------------|-------------|
| – Max possible | 250 lm/W | | |
| – Tungsten | 16 lm/W | <0.01 \$/W | 1,000 hrs |
| – Flourescent | 60 lm/W | | 8,000 hrs |
| – LED | 50-80 lm/W | 2-5 \$/W | 50,000 hrs* |

*Depends a great deal on keeping it cool !

Total cost of ownership works today (energy + replacements) – but we are not good at making long term financial decisions !!

Applications

- High replacement cost, leverage life
 - Traffic lights
 - Commercial lighting
- Leverage design
 - Car lights
- Low power, leverage efficiency
 - Cell phone display
- What's next
 - Home, leverage design & efficiency
 - Projection displays leverage brightness of LED with photonic crystals
 - FPD, leverage color control



RGB Edge Lighting LED's for Flat Panel Illumination



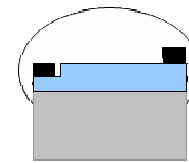
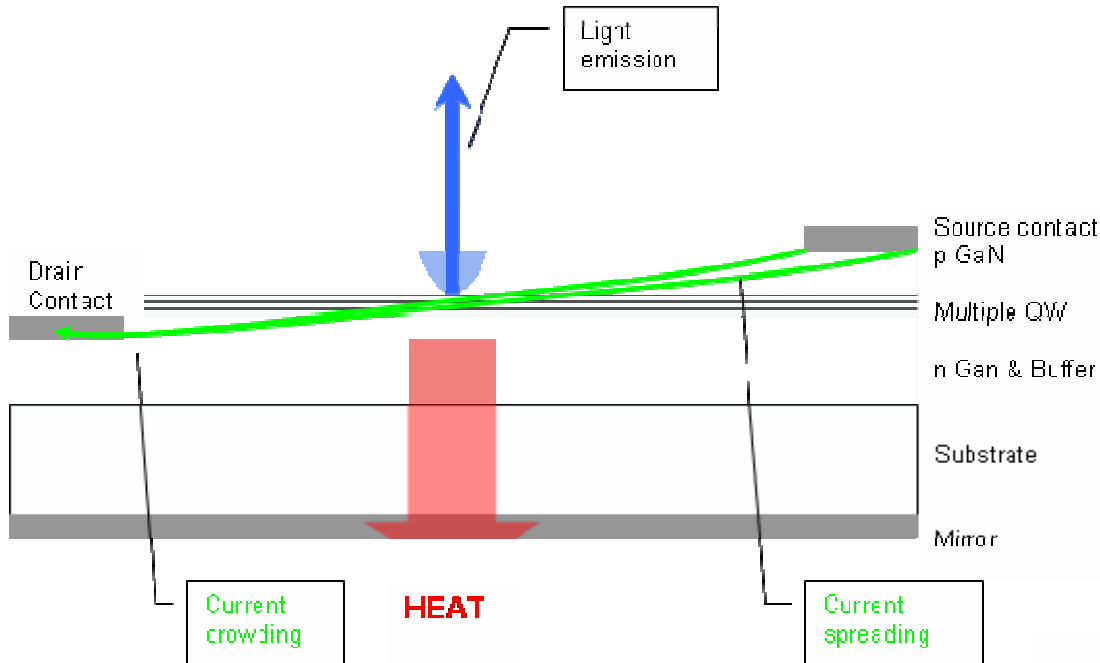
15" Diagonal
Screen
2500 lumen
120W
18,000 nits
LEDs
24 Green
8 Blue
32 Red



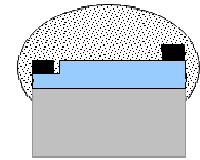
How does nanotechnology help ?

- The problem and conventional solutions
- Light extraction
 - Photonic crystals + thin devices
- Light creation
 - + reflectors + webbed conductors + patterned growth

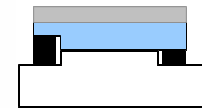
An LED



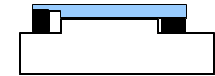
a) Encapsulated standard LED



b) Phosphor loaded encapsulant for white LED

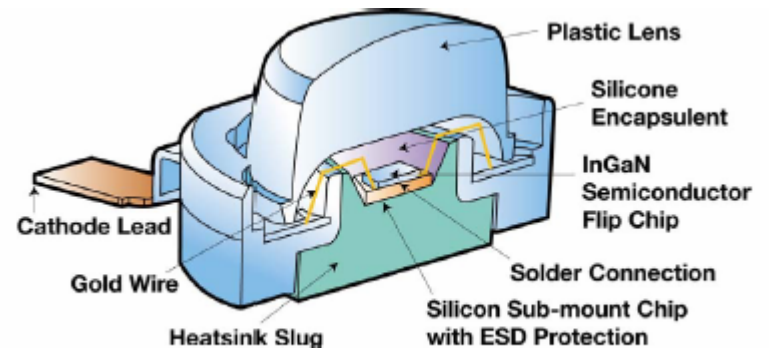


c) Flipped LED with thinned substrate



d) Ultra thin LED with substrate and GaN removed at a separation layer

Device options



Cross section view of Luxeon Emitter

Structure of a Light Emitting Diode

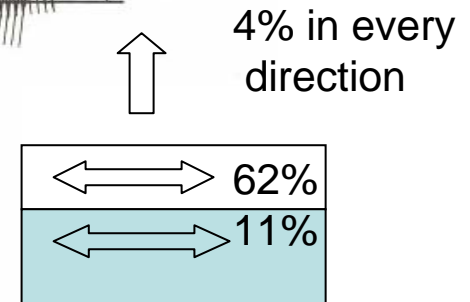
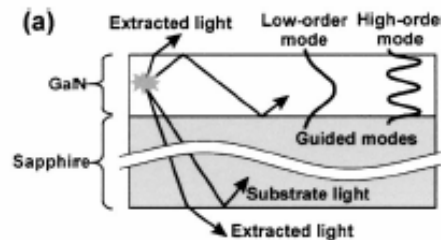
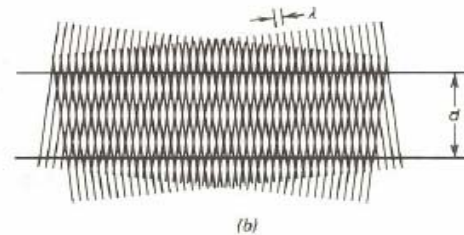
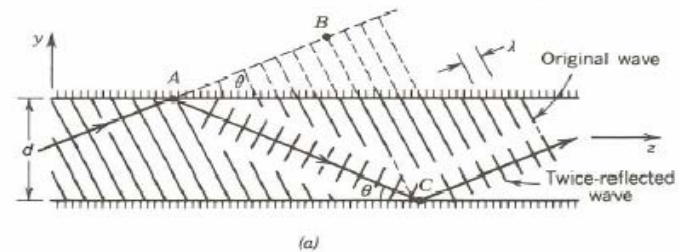
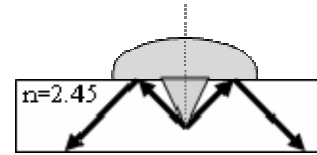
Light trapping

GaN layer has a high refractive index, a limited angle of light leaves, the rest undergoes Total Internal Reflection

Multiple bounces “interfere”

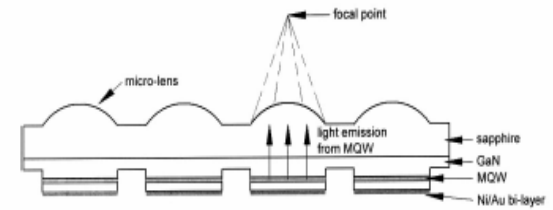
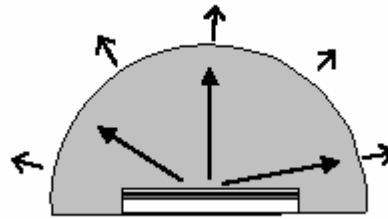
Creates standing waves – waveguide modes

62% of light is trapped in GaN layer
11% trapped in substrate

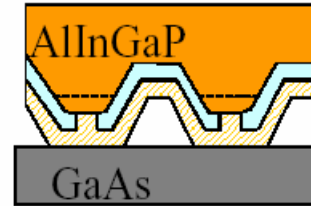
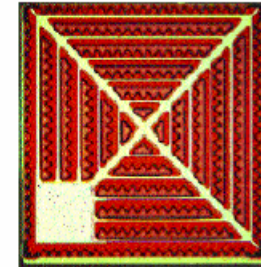
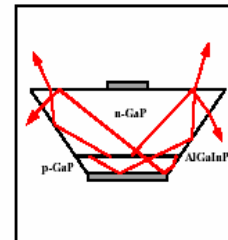
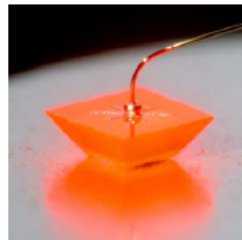


Conventional Solutions

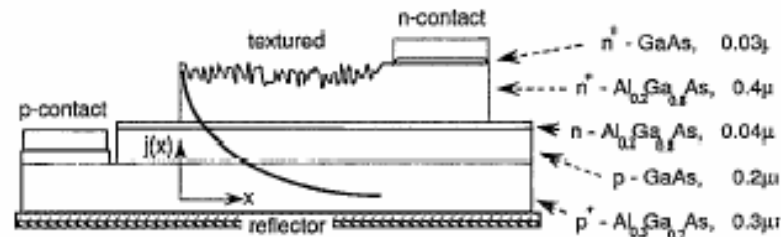
- Encapsulation
 - traditional



- Faceting
 - Very expensive



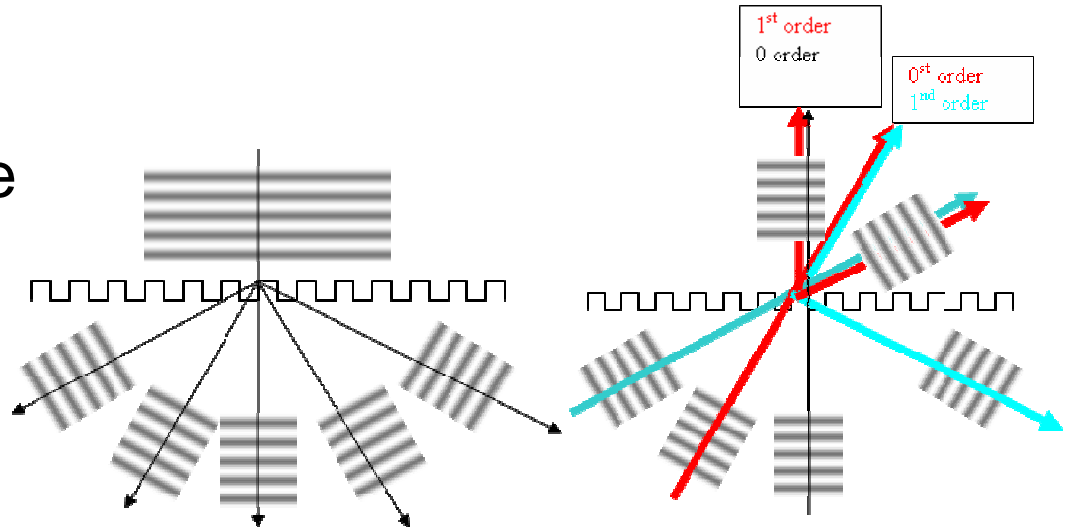
- Roughening + encapsulation
 - Industry standard



Patterned extraction

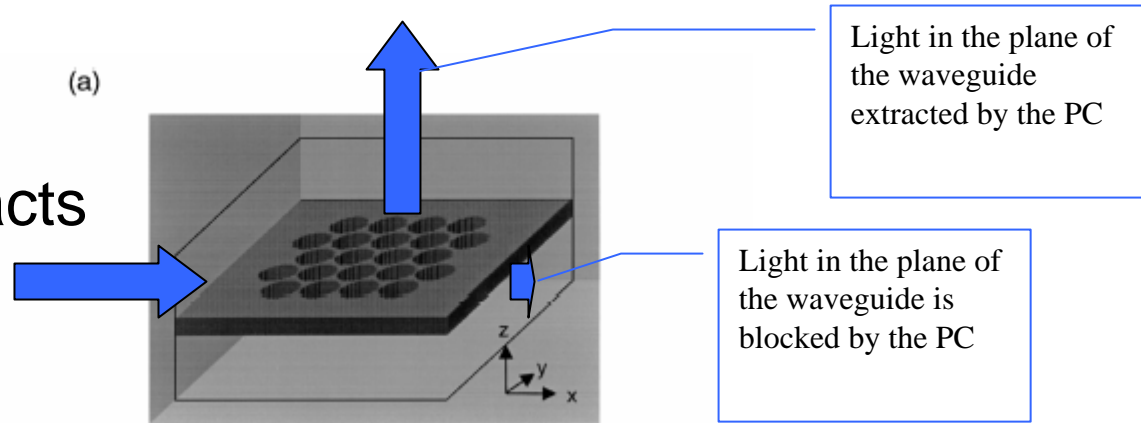
- Gratings

- Pattern on surface
- Directs light

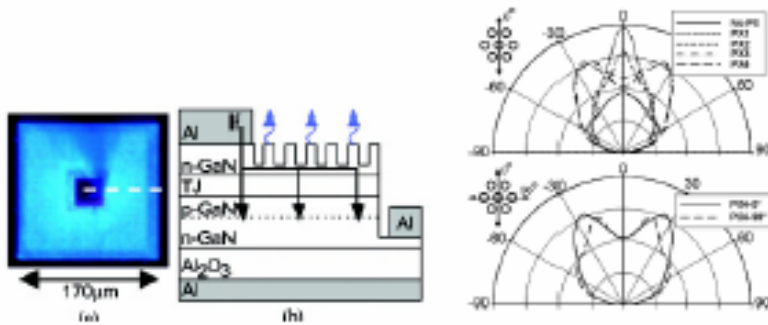


- Photonic Crystals

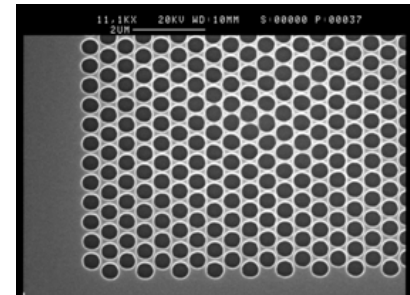
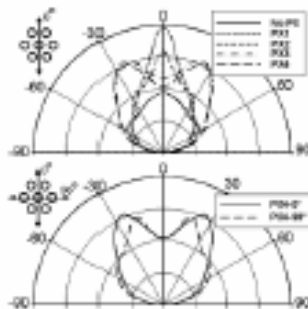
- Pattern through waveguide
- Absorbs and extracts light



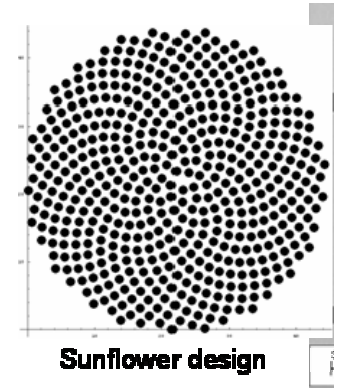
Photonic Quasi Crystal optimizes beam shape and uniformity



Lumileds showed beam shaping experimentally
Luminus Devices are selling product for projection displays



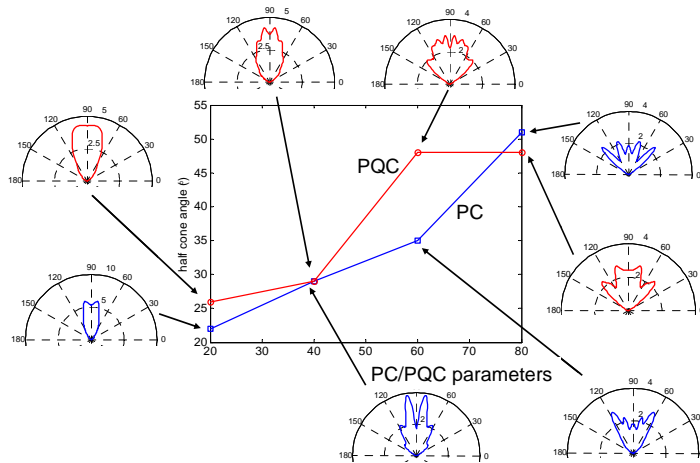
Regular PC



Sunflower design

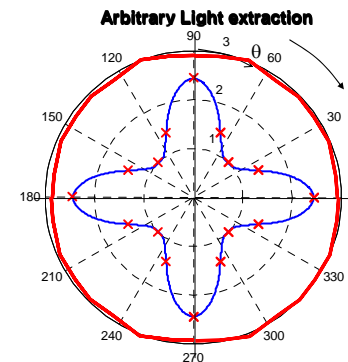
Photonic Quasi Crystal

Below – radial light distribution

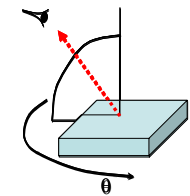


Mesophotonics showed beam shaping control in models

— Photonic quasicrystal (PQC)
— Photonic crystal (PC)



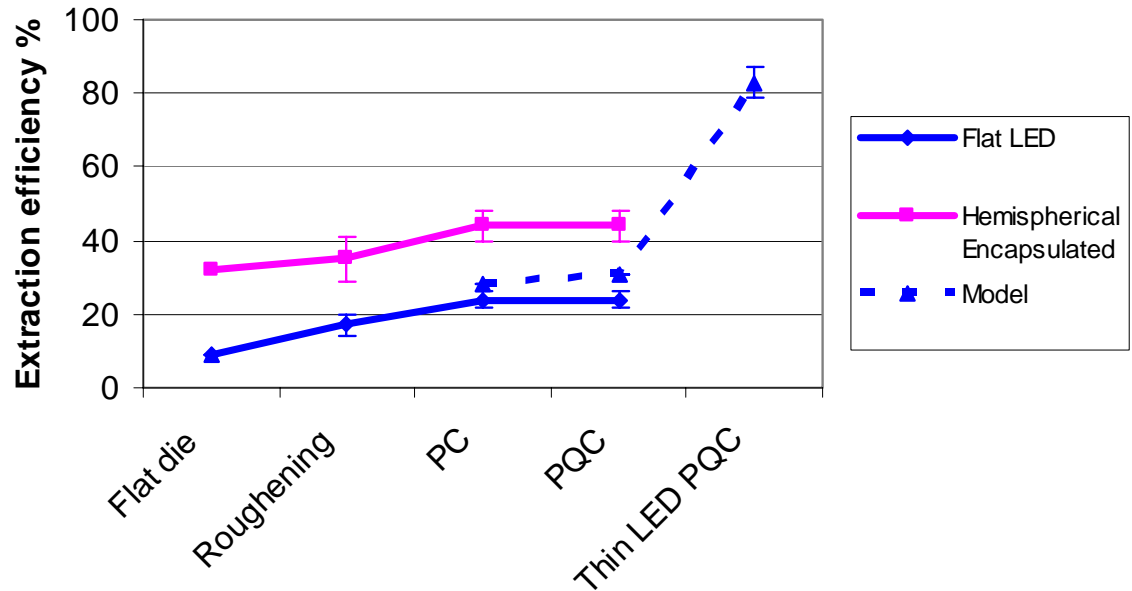
Simulation assuming viewer integrating light between altitude angle=0 to 90°



Pitch = 300nm
Hole diameter = 120nm
Etch depth = 150nm

PC control of extraction

- Roughened encapsulated devices have 30-40% extraction, consistent with 50-80 In/W devices
- Encapsulated PQC 45% > roughening 35% or 1.25x improvement
- Thin device 80% > thick 45%
- Model matches experiment (carefully optimized examples)



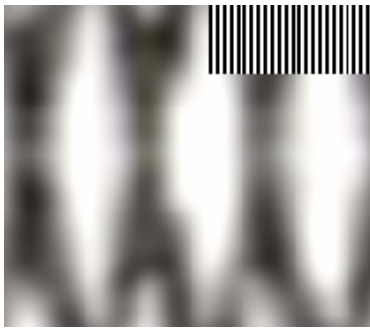
Model and experimental data showing control of the light distribution by the photonic crystal, from literature and Mesophotonics. Literature data “normalized” to a 3um thick GaN device. Effect of encapsulation on roughened devices scaled from PC.

PC and thin devices

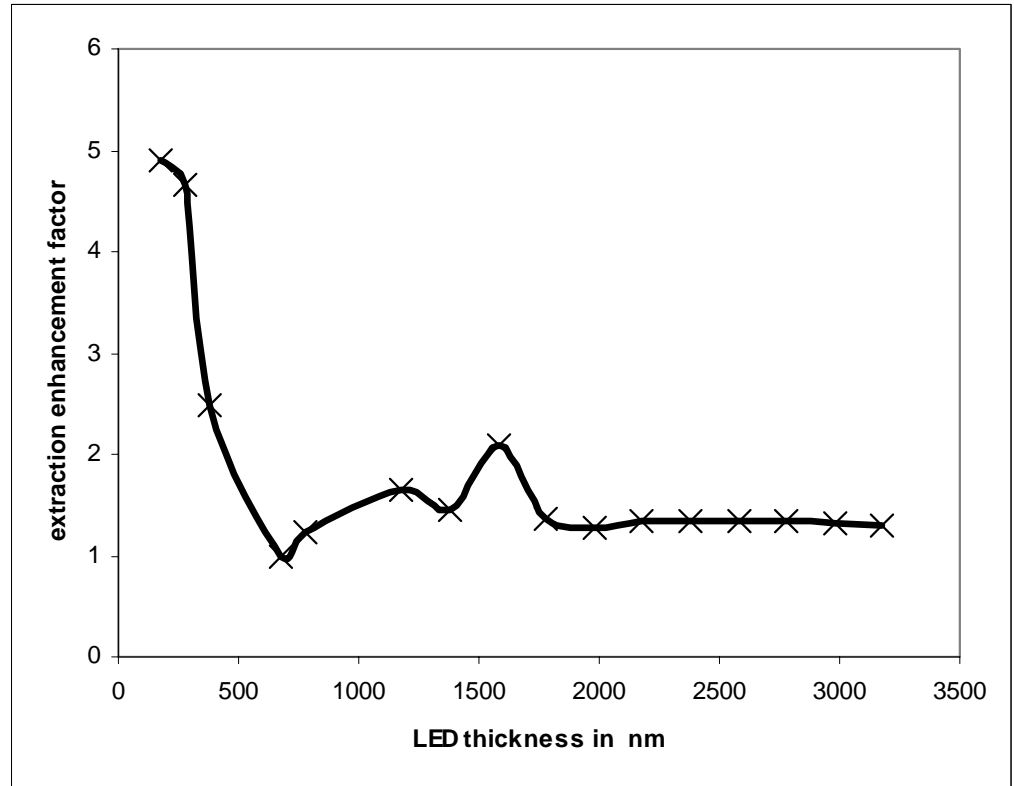
0.5 μm



1 μm



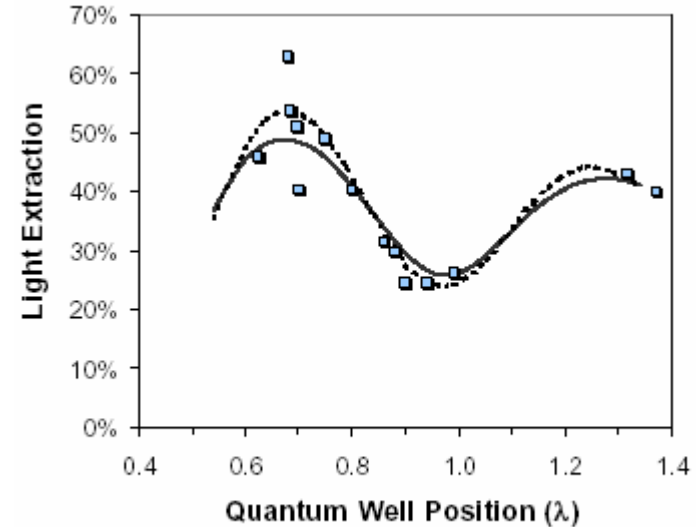
More PC overlap with modes in a thin LED, hence better extraction



Model data for LED optimized at 3 μm thick and then thinned. *Mesophotonics*.

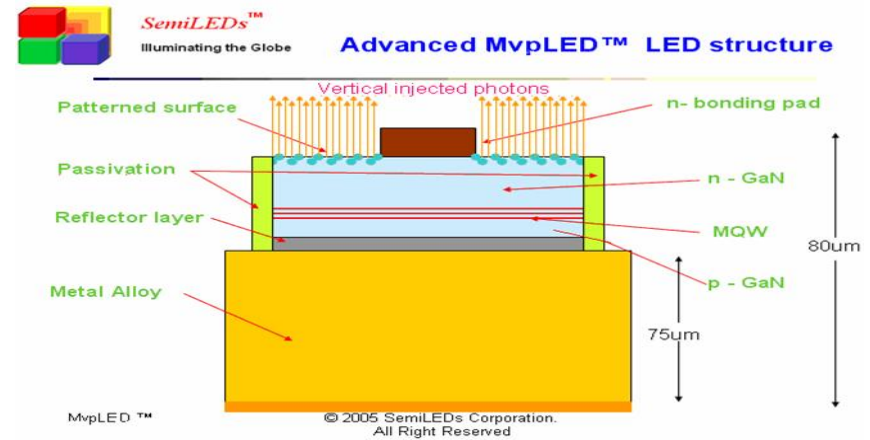
Light creation – effect of adding a mirror

Mirror placed close ($< 1 \lambda$) to quantum well maximizes output
Lumileds

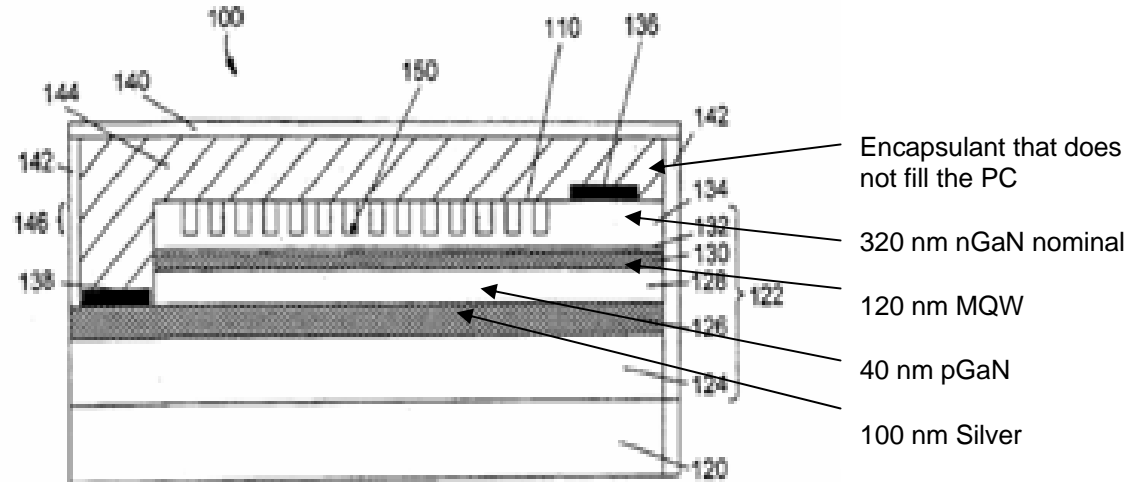


Shen et. al., *Appl. Phys. Lett.* **82**, 2221 (2003).

Metal substrate can act as mirror and heat sink
Semileds



Optimized thin (<math><0.5 \mu\text{m}</math>) devices



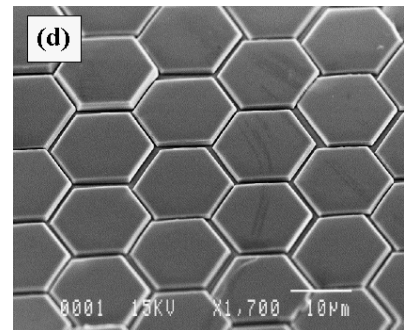
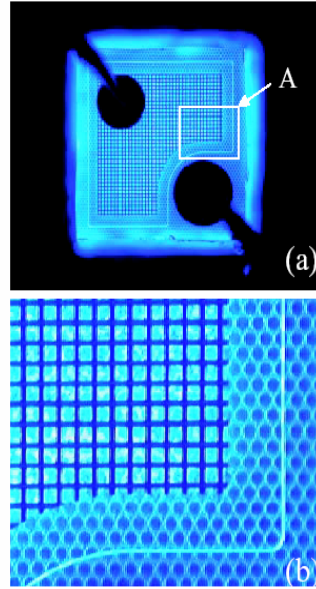
Regular lattice, pitch from 200 to 300 nm
 Regular lattice, varying fill factor
 Regular lattice, randomized pitch by 10%
 Pattern optimization
 Quasi crystals

57- 69%
 57/60/54 %
 70%
 73-80%
 83%

Luminus Devices Patent Specification

Light creation

- Web of conductors
 - Control current distribution
 - Nichia have implemented
- Lateral overgrowth
 - Grow through holes patterned in substrate
 - Reported by all major suppliers



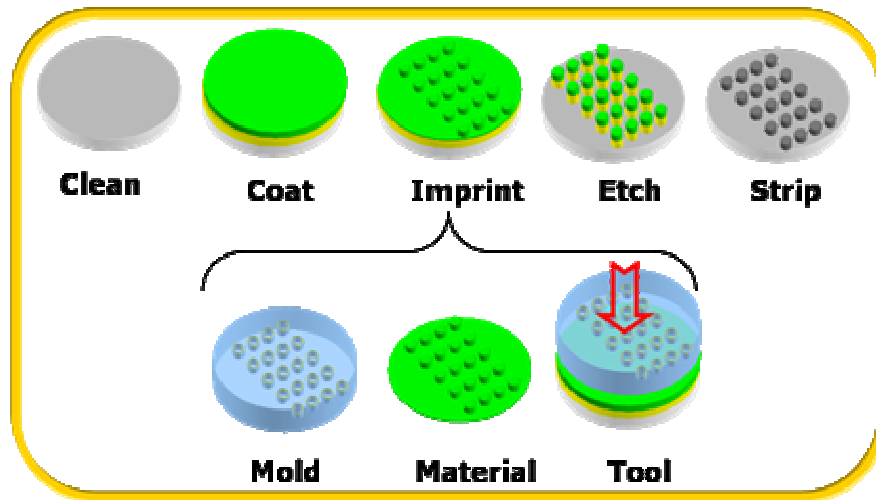
Future device

- Grown by lateral overgrowth
- Mirror deposited
- Surface sub micron layer sliced off / thinned and flipped
- PQC patterned
- Extraction potential > 80%
- Reduced cost
 - Brighter than florescent, reduced heat sinking
 - All wafer level processing
 - Large die, fewer packages
 - Simple package
 - Processed in automated factory > 3" wafers

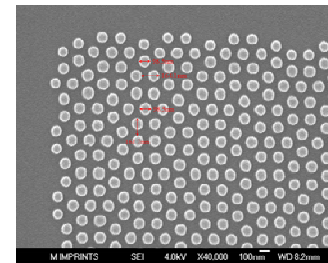
How to implement nanotechnology cost effectively ?

- | - Requirements LED | Integrated Circuit |
|---|---------------------------|
| - Sub 100 nm features at < 1 c per device | 50 c per device |
| - Limited overlay 2-3 um | 20 nm overlay |
| - Redundant part not defect critical | 1, 20 nm defect is lethal |
| - Imperfect wafers | Perfect wafers |
-
- Solutions
 - Optical – horribly expensive (\$20M)
 - Electron beam – expensive (\$5M) and slow
 - Imprint – ideal application (\$1-2M)
 - How does imprint work ?
 - Which companies are poised to make an impact ?

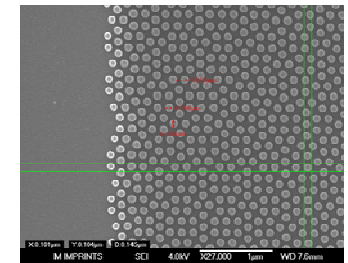
Imprint module



12F Quasi 2 Array



Wafer 14; CD = 99 nm



Wafer 524; CD = 104 nm



a) EVG clean coat system

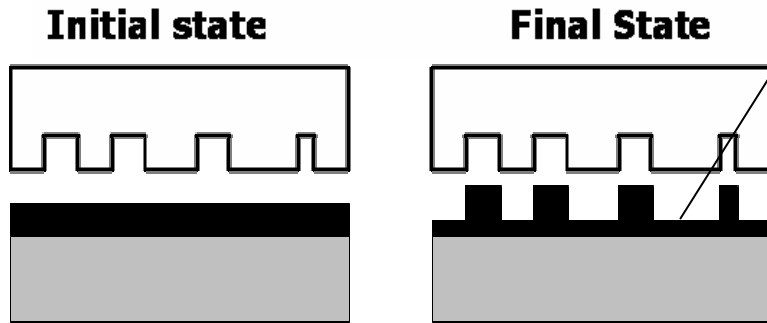


b) MII imprinter

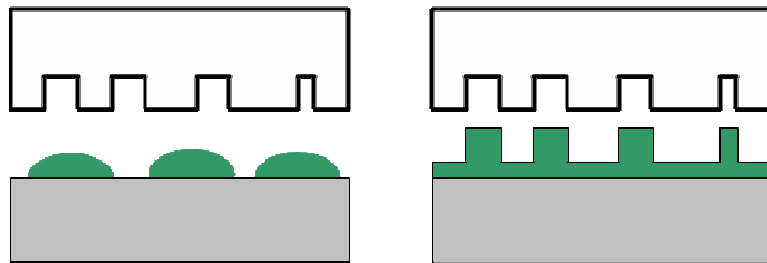


c) Trion etcher

Imprinting

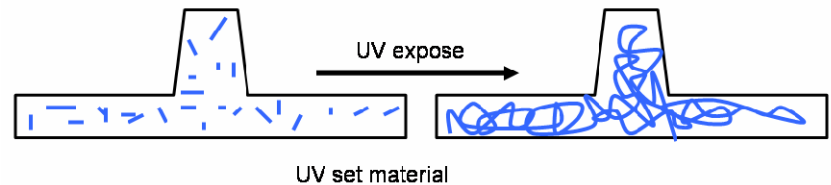
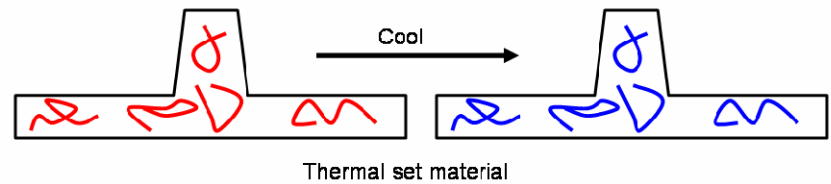


Thermal or UV imprint of a spin on layer



UV imprint of a drop dispense material

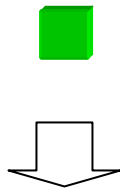
Residual layer, must be \ll pattern height, around 50 nm



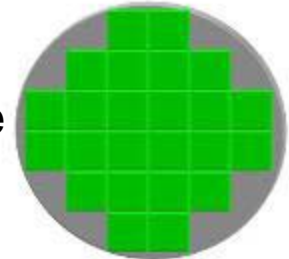
UV cure is faster than thermal
Industry consensus

Making the mold

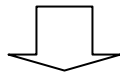
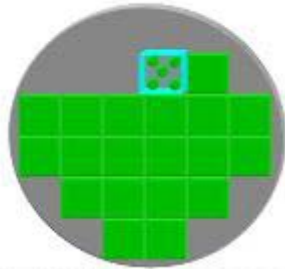
Electron beam write
a few die, etch the pattern



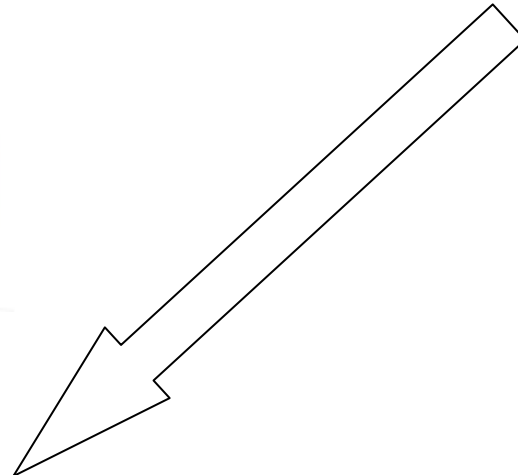
Electron beam write
a whole mold, etch the pattern



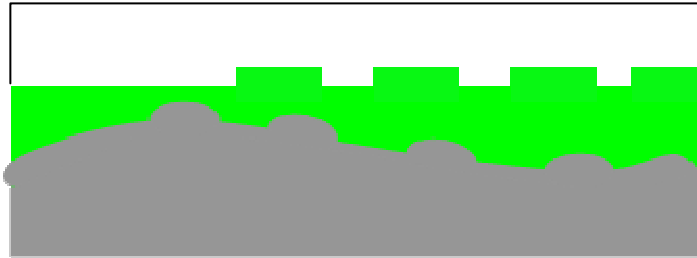
S&R imprint whole
mold



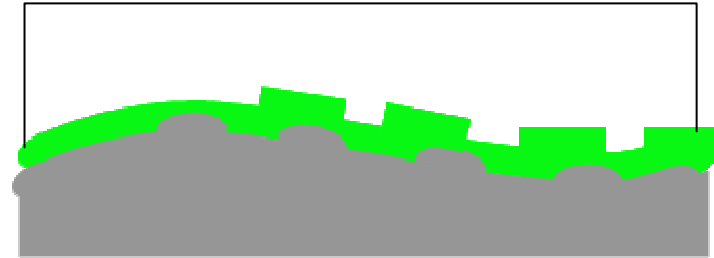
Use or make
multiple copies –
“working plates”



Imprint on rough wafers

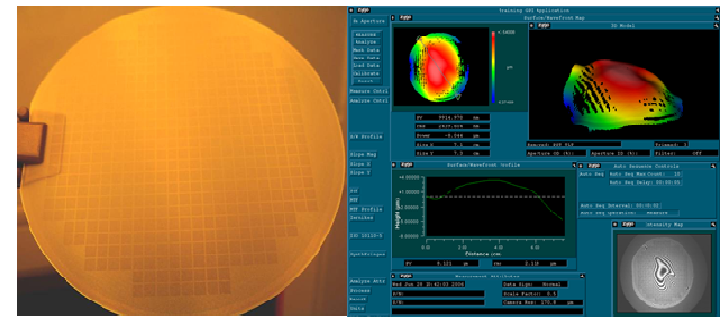


Non – conformal



Conformal - mold deforms

- Flex wafer
 - Contact printer solution, **not sufficient for LED wafers**
- Flex thin hard mold; MII, Nanonex
 - **Hard surface is cleanable, lowest cost of ownership**
- Soft plastic, fragile mold
 - either need **many working copies, highest cost** - EVG
 - or have a **“one use mold”** – a **dual head imprinter** – Obducat
- **Mold or imprint must be monitored in all cases**



8 um flat wafer
9 nm uniform imprint
MI

Production imprint solutions

All production tools are in varying stages of development, all should be made to work.

- EVG
 - Supplies converted contact printer
 - > \$200 M in sales
 - “Production system available ARO”
 - Make your own soft working mold
- MII
 - Reported most performance data
 - Supplies thin hard molds, and supports master creation and detailed process applications
 - Production tool focus
 - Best throughput potential
 - Start up
- Nanonex
 - Dominates manual lab tools
 - “Production system available ARO”
 - No mold technology recommendation
 - Start up
- Obducat
 - Second manual lab tool supplier
 - Small public company
 - Developing first production “one use mold” system
 - Limited overlay from plastic film mold
- Numerous minor suppliers; Suss etc.

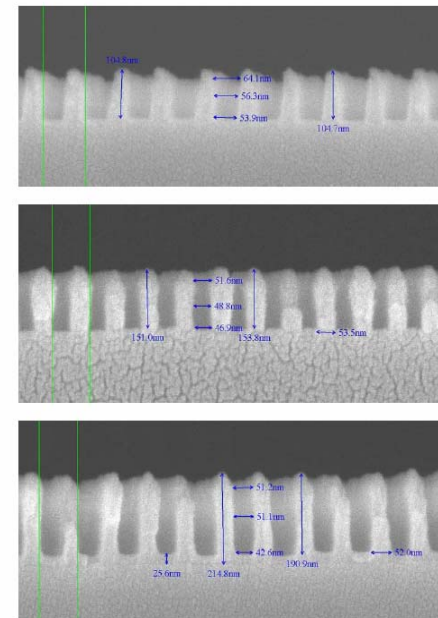
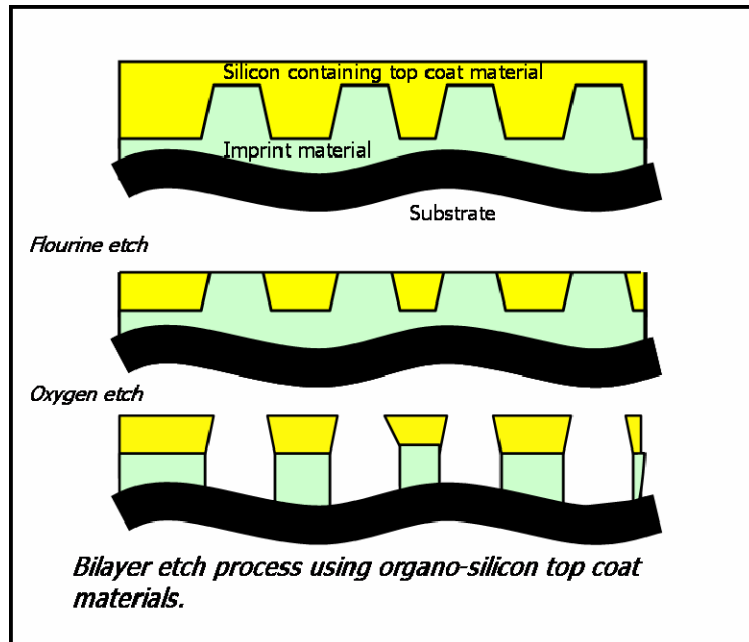


b) MII imprinter

Process

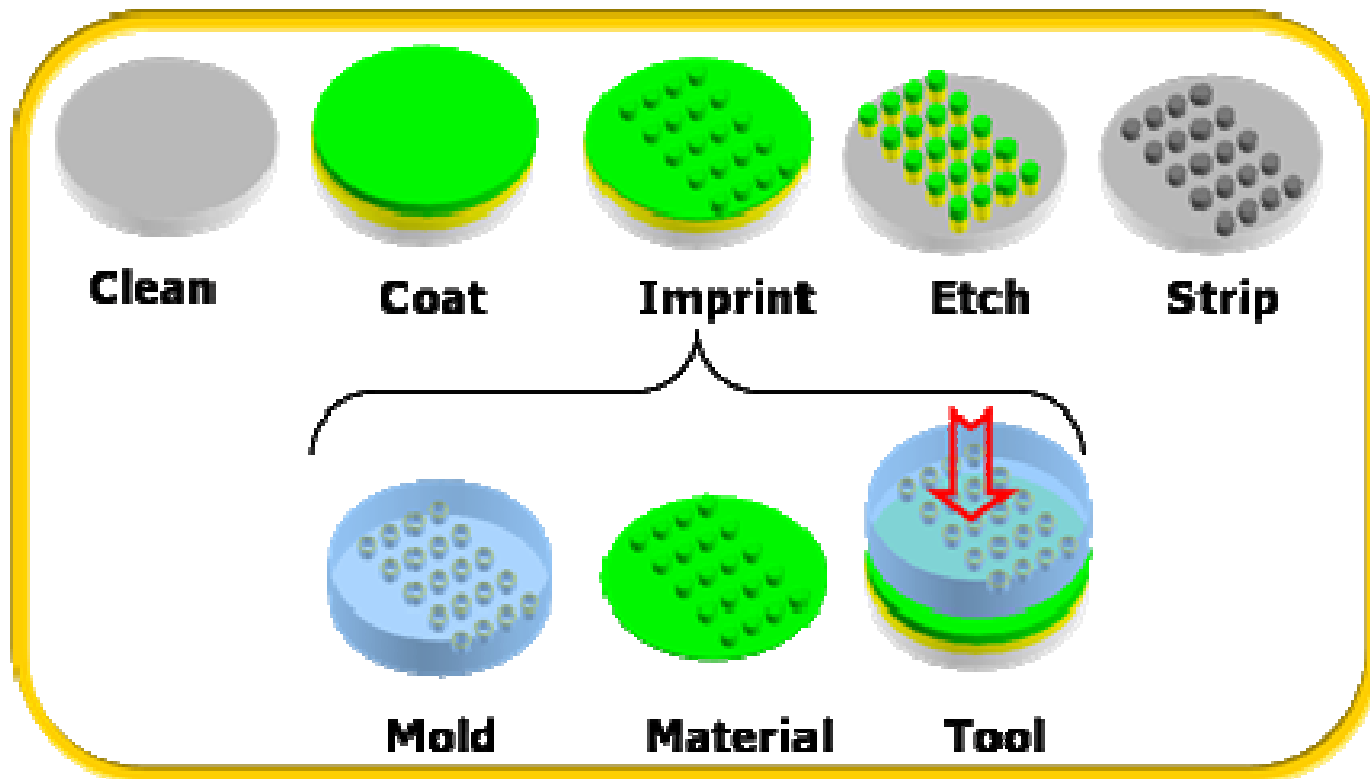


To pattern over small length scale roughness
need planarization



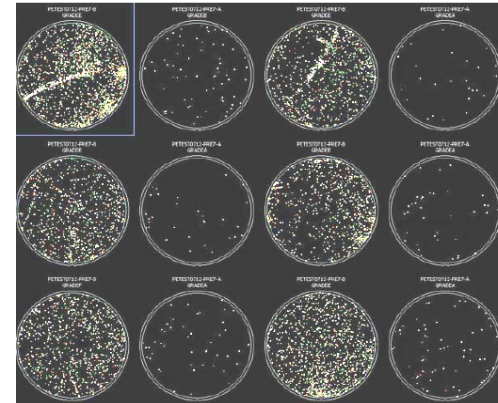
50 nm features – 100 nm height change
MII

Rest of the module



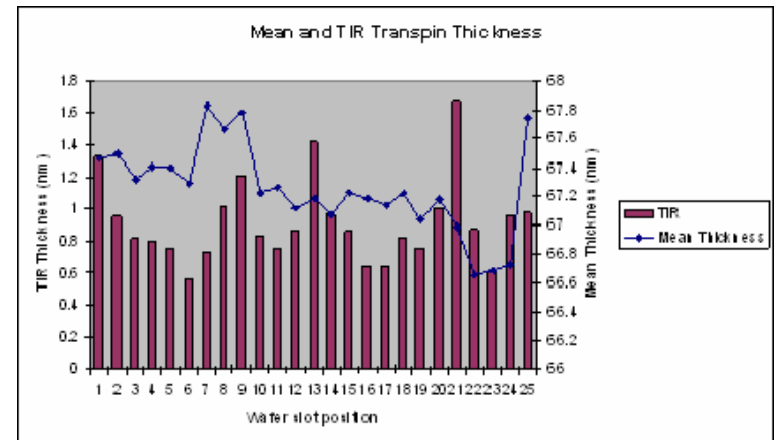
Clean and Coat

- Requirements < 50 nm residual layer thickness on 150 nm planarization layer
 - < 10 particles per wafer greater than 100 nm
 - < 10 nm variation in thickness
 - Small wafers



Pre Post Pre Post
Clean data from SSEC, < 8 particles post clean

- Suppliers should meet these targets
 - EVG
 - Suss
 - SSEC
 - S-Cubed



Coat thickness data on a S-Cubed systems, < 5 nm variation

Etch

Multiple etch steps

1. Residual layer
2. Planarization
3. Hard mask
4. GaN – needs high density plasma

Suppliers of multichamber systems,
support GaN etch on small wafers

Trion

Oerlikon (used to be Unaxis)



GaAs etch



c) Trion etcher

Metrology

- Defects
 - The regular pattern makes defects much more visible
 - KLA patterned wafer Surfscan
 - KLA optical inspection
- Thickness < 50 nm
 - Spectrometry – Metrosol (Austin TX)
 - Ellipsometry – KLA, Nanometrics
- SEM
 - Phillips
 - Jeol
 - Hitachi
- Used equipment available in most cases

Cost of ownership

- Price of systems and materials will tend to converge due to competition
- Mold life and cost to replicate will be the dominant cost differential between suppliers solutions.
- Imprint module COO is in the \$10-15 a wafer range – 5,000-8,000 die per wafer

Conclusions

- Nanopatterning poised to impact LED's
 - Luminus Devices have implemented PC on LED by imprint and you can buy a projector today !!
 - Photonic Quasi Crystals offer uniform light beam essential to avoid external optics
 - Photonic Crystals on Nanolayer devices have potential for 80% extraction
 - Web conductors
 - Overgrown epitaxy
- Imprint poised to enable manufacturing
 - 2 suppliers are developing production solutions - MII , Obducat
 - 2 suppliers have committed to build to order – EVG, Nanonex